

# SPECIFICATION

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## WRITEBACK AND REFRESH CIRCUITRY FOR DIRECT SENSED DRAM MACRO

### Background of the Invention

[0001] 1.Field of the Invention

[0002] The present invention relates generally to writeback and refresh circuitry for a direct sensed DRAM macro, and more particularly pertains to writeback and refresh circuitry for a direct sensed DRAM macro wherein bitline data is sensed with a primary sense amp (PSA) without a storage means, and then the data is transferred to a latch in a secondary sense amp (SSA) which is common to a group of direct sense memory arrays. A single MDQ master data line is used to first carry the read data as an analog level signal to the SSA, which digitizes the data and then returns the digitized data over the same MDQ global data line as a full-rail digital signal back to PSA and the memory array bitlines.

[0003] 2.Discussion of the Prior Art

[0004] Direct sense memory arrays are memory arrays wherein only the gate of the sense device/transistor is connected to a sensed bitline BL, such that the sense device does not provide any feedback to or alter the signal on the sensed bitline BL. This is in contrast to other prior art nondirect sense memory arrays which include a cross coupled latch wherein typically both the gate and the drain of a sense device/transistor are connected to a sensed bitline BL, and wherein the sense device provides feedback to and alters the signal on the sensed bitline BL.

[0005] Direct sense memory arrays typically use a dense and high speed primary sense amp (PSA) which does not latch sensed data during a read operation, and the sensed

data is typically directed to an external cache, from which it is written back into the memory array during a refresh operation, which is a very time consuming operation and also requires the use of the external cache which could otherwise be performing other functions in the system. As such, an accessed memory storage cell does not get directly written back, or restored, after a read operation, but rather has an indirect writeback or restore operation.

[0006] In a typical nondirect prior art direct sense memory array, data is stored in a latch in the PSA, and is then directly written from the PSA into a memory storage cell. In contrast thereto, in the present invention data is stored in a latch in the secondary direct sense amp (SSA) where it is further amplified and stored as a true digital signal, and is then written directly from the SSA into a memory storage cell.

## Summary of the Invention

[0007] Accordingly, it is a primary object of the present invention to provide writeback and refresh circuitry for a direct sensed DRAM macro wherein bitline data is first sensed with a primary sense amp (PSA) without a storage means, and then the data is transferred to a latch in a secondary sense amp (SSA) which is common to a group of direct sense memory arrays. A single MDQ master data line is used to first carry the read data as an analog level signal to the SSA, which digitizes the data and then returns the digitized data over the same MDQ global data line as a full-rail digital signal back to the PSA and the memory array bitlines.

[0008] The present invention provides a circuit for performing a write operation, and a 2-cycle read-write refresh operation to refresh a dynamic eDRAM direct sense memory array. The PSA reads the data and then transfers the data to a shared SSA along a shared MDQ global data line. The SSA converts the analog data to digital data with a resistive isolation device and a latch with weak feedback. The resistive isolation device and a read current supply in the SSA are then shut off, after which a feedback device in the SSA is enabled to pass the inverted and amplified data back to the array cell over the shared MDQ global data line.

[0009] The present invention provides a read/writeback mechanism in a destructive read memory array wherein 2-cycles are used for each memory read cycle, a first cycle read

operation, and a second cycle writeback operation. The 2-cycle destructive read architecture eliminates the need for a cache and complex caching algorithms.

## Brief Description of the Drawings

[0010] The foregoing objects and advantages of the present invention for a writeback and refresh circuitry for a direct sensed DRAM macro may be more readily understood by one skilled in the art with reference being had to the following detailed description of several embodiments thereof, taken in conjunction with the accompanying drawings wherein like elements are designated by identical reference numerals throughout the several views, and in which:

[0011] Figure 1 illustrates a Write-Refresh circuit for a direct sense memory architecture pursuant to the present invention.

[0012] Figure 2 illustrates a primary direct sense amp (PSA) pursuant to the present invention as can be used in the circuit of Figure 1.

[0013] Figure 3 illustrates a secondary direct sense amp (SSA) pursuant to the present invention as can be used in the circuit of Figure 1.

[0014] Figure 4 illustrates the timing of waveforms used to perform a 2-cycle refresh, or writeback, of both "1" and "0" data.

[0015] Figure 5 illustrates a PSA with a local writeback wherein the sensed/read data is written back through the PSA with an inverted write path

## Detailed Description of the Invention

[0016] Referring to Figure 1, an array of dynamic memory storage cells C are connected to a plurality of primary direct sense amps (PSAs), each of which can comprise the circuit of Figure 2. The outputs of the plurality of primary PSAs are connected to a single secondary direct sense amp (SSA), which can comprise the circuit of Figure 3, through a common MDQ global data line. The basic direct sense read operation is described in U.S. Patent Application Serial No. 09/870,755, filed May 31, 2001 and entitled Single Bitline Direct Sensing Architecture.

[0017] Figure 2 illustrates a PSA pursuant to the present invention as can be used in the

circuit of Figure 1. The PSA includes:

[0018] a pair of precharge/equalize PFET devices T0, T6 coupled between a power supply Vdd and the respective bitlines BL, BBL, which are coupled to memory storage cells C which are selected for write and read operations by a plurality of wordlines WLn;

[0019] a pair of write switch NFET devices T12, T11 coupled respectively between the bitlines BL, BBL and the MDQ global data line;

[0020] a pair of read NFET devices T15, T17 coupled respectively between the bitlines BL, BBL and the MDQ global data line;

[0021] a pair of read enable/switch devices T14, T16 coupled in series respectively with the read devices T15, T17 and ground, all of which are connected as shown in Figure 2.

[0022] During a read operation of a data 0 the devices T15, T17 convert a read signal of tens of millivolts on the bitlines BL, BBL to a signal of hundreds of millivolts on the MDQ global data line. The PSA uses write devices T12, T11 which are NFET devices operated with a boosted gate level signal WRT, WRC, which is a denser design relative to circuits which use a pair of complementary transistors.

[0023] Figure 3 illustrates an SSA pursuant to the present invention as can be used in the circuit of Figure 1. The SSA comprises:

[0024] a current I supply PFET device T4 connected in series with an enable/switch PFET device T25, which are connected between a power supply Vdd and the MDQ global data line, and during a read operation of a data 1, the read devices T15, T14 of the PSA are turned on and connect the MDQ global data line to ground, and the current supply devices T4, T25 function similar to a resistive voltage divider network to allow the global data line MDQ to proceed to ground;

[0025] a horizontal resistive isolation NFET device T2, biased to operate in its linear range of amplification, coupled between the MDQ global data line and an inverting latch which isolates/decouples the global data line from the inverting latch;

[0026] a cross couple inverting latch, coupled to the output of the resistive isolation

device T2, and comprising latch output devices T1, T5, and feedback devices T3, T28 which provide a weak feedback signal such that the latch is stable in a first state but is more stable in a second state, such that it is more easily switched from the first state to the second state than vice versa, to provide a hair trigger type of switching operation;

[0027] a precharge device T31 coupled between the power supply Vdd and the input to the latch; a pair of invertors inv\_0, inv\_1, coupled between the output of the latch and an output node ssa\_out, to provide buffering therebetween and also to convert the latch output signal to a signal at ground for a data 0 and at full rail voltage of approximately 1 volt for a data 1;

[0028] an open drain, pull down and inverting device T\_OUT connected between the output node ssa\_out and a data\_out line;

[0029] a refresh/rewrite device T50, connected between the output node ssa\_out and the MDQ global data line, which is turned on during a refresh/rewrite operation to rewrite data back into the memory array;

[0030] a data write device T\_IN, connected between a data\_in line and the MDQ global data line, which is turned on during a data write operation to write data back into the memory array.

[0031] During a read operation, a data 1 in a memory cell translates through the SSA circuit of Figure 3 to a full rail high signal at approximately 1 volt at node ssa\_out, which during a read operation is inverted to an opposite polarity data signal on data\_out, and during a writeback operation is read as a data 1 at node ssa\_out by refresh device T50.

[0032] Referring collectively to Figures 1, 2 and 3, during a write operation, the data\_in line drives the SSA, in which the data write device T\_IN is activated by a write signal WRSSA, and its output is directed to the common MDQ global data line. The common MDQ global data line drives the plurality of PSAs. A pair of PSA write switches, having inputs of WRT and WRC of Figure 2, are decoded in on or more selected PSA(s), as selected by a WRT/C signal on a bus from the Read Write Control, and direct the incoming data to the proper bitline and memory storage cell. The bitlines were initially

precharged to a high level  $V_{blh} = V_{dd}$  at the end of the previous cycle, such that in the PSA a single NFET device T12 or T11 with a boosted WRSSA level is sufficient to write a "1" or a "0" data level to the bitline and the selected storage cell, which is selected by the Word Decode/Control which activates a selected Word Driver to write the data into the storage cell activated by both the selected wordline  $WLn$  and the selected PSA.

[0033] During a read operation, the read data is amplified in the following manner. The PSA of Figure 2 connects the bitlines BL, BBL directly to the gate of a data sensing FET, T15 for BL, T17 for BBL. The data level on the bitline determines a corresponding data level on the MDQ global data line which is driven by the outputs of T15 and T17, and which is connected to both the current load device T4 and the resistive isolation device T2 of the SSA of Figure 3. The resistive isolation device T2 passes the MDQ global data line signal to precharged latch devices T1, T3, T5 and T28, which are precharged by device T31, and the latch latches and inverts the input signal MDQGATE. Additional buffering is provided by serially connected inverters  $inv\_0$  and  $inv\_1$  at the output of the latch, which also provide a full rail data 1 or 0 at the node  $ssa\_out$ , which drives the output device T\_OUT, the inverted output of which drives the data\_out line. The data\_out line has a relatively large capacitance, such that the device T\_OUT is rather large, and the inverters  $inv\_0$  and  $inv\_1$  buffer the inverting latch from the large capacitance of the device T\_OUT is activated.

[0034] As an example, assume a read operation of a data 1 from a memory storage cell connected to bitline BL and activated by the selected wordline  $WLn$ . The bitline BL is initially precharged by precharge device T0, and a read data 1 on the bitline causes the bitline to remain at the precharge level, which fully turns on device T15. Device T14 is also activated, connecting MDQ through T14, T15 to ground and causing the signal voltage or MDQ to drop, which is the input signal to the SSA. In the SSA, the drop in MDQ causes resistive device T2 to produce a lower output, such that MDQGATE goes to essentially ground, such that the latch, which has also been precharged, inverts and produces a latch output signal of 1. The data\_out line is also precharged high to  $V_{dd}$ . The inverters  $inv\_0$  and  $inv\_1$  provide a full rail high output signal of approximately 1 volt at node  $ssa\_out$ , which turns device T\_OUT on to connect the data\_out line to ground therethrough, such that data\_out line drops from

its precharge level toward ground, such that an inverted data signal is produced on the data\_out line.

[0035] A read data 0 on the precharged bitline BL causes the BL signal to drop, which limits the turn on of, and only partially turns on, the device T15, such that MDQ does not drop as much as for a data 1, but drops to a voltage level of several hundred millivolts, such that the device T2 in the SSA passes a higher signal to the input MDQGATE of the latch, causing the inverting latch to latch to a data 0, such that the inverters inv\_0, inv\_1 produce a true digital data 0 output signal at output node ssa\_out, which does not turn device T\_OUT on, causing the line data\_out line to remain at its precharge level to produce an inverted data signal on the data\_out line.

[0036] Following a destructive read operation, for a writeback of the data signal, in the SSA the devices T2 and T25 are turned off, and then the refresh device T50 is turned on by a boosted gate signal RFSHd. In the case of a data 1, this causes a full Vdd to pass through device T50 to charge MDQ to Vdd. In the PSA, device T12 or T11 is turned on to write the data 1 to bitline BL or BBL. In the case of a data 0, a ground level 0 voltage signal passes through device T50 to pull MDQ to ground. In the PSA device, T12 or T11 is turned on to write the data 0 to bitline BL or BBL.

[0037] A write operation proceeds in a manner similar to a writeback operation, but instead of activating refresh device T50, write device T\_IN is activated to write the data on the data\_in line back into the memory array.

[0038] The primary and secondary direct sense amps as described above differ from prior art nondirect read architectures which perform the data latching and writeback operations in the PSA rather than in the SSA, as in the present invention. The present invention is more efficient from a circuit area viewpoint as a memory array includes many more primary DSAs than secondary DSAs.

[0039] A 2-cycle memory write/refresh operation can be performed in the direct sense architecture of the present invention by first transferring the data from one array in the memory bank to a multiplexed SSA in a first memory read cycle. In a second cycle, the devices T2 and T25 are shut off, and the device T50 is then activated, and the amplified read data is directed back to the PSA in a refresh operation as described

above. This is best accomplished by leaving the wordline active for both of the 2-cycles, with no wordline restore between the read and write/refresh operations. The return path device T50, with its gate connected to a RFSHd signal, is used to connect the amplified ssa\_out data node signal back to the MDQ master data line.

[0040] Figure 4 illustrates the timing of waveforms used to perform a 2-cycle refresh, or writeback, of both "1" and "0" data. The bitline can be precharged/restored to its  $v_{blh} = V_{dd}$  level before the writeback for an improved "1" level, or alternatively the bitline EQ could be inhibited for an improved "0" writeback, with a circuit designer being able to choose either option. Note in Figure 4 that both a data 1 and a data 0 are rewritten into the memory storage cell at an improved respectively higher and lower signal level than the original read data 1 and data 0.

[0041] Figure 5 illustrates an alternate embodiment wherein inverted digitized data is fed back onto the bitlines without the use of a cross coupled storage latch. Write data\_in is pre-inverted and sent up the MDQ master data line from external sources, and read data is inverted and directed through the same write devices (WRT, WRC) as used in the external write path.

[0042] Figure 5 illustrates a PSA with a local writeback wherein the sensed/read data is written back through the PSA with an inverted write path. It should be recalled that the data level on the MDQ global data line is inverted, being low for a data 1 and high for a data 0. Accordingly, in this alternative embodiment, the level on the MDQ master data line is digitized and inverted by one of two additional inverters, inv\_2 for bitline BL, and inv\_4 for bitline BBL. The Vdd power supply lines for these inverters can be switched off during a read operation, and powered on during a write operation. Similar to the PSA of Figure 2, the WRT or WRC control gates of respective devices T23 and T13 are activated after a read operation to perform a direct writeback of data back to the storage memory storage cell. The inverters are designed with beta ratios similar to the beta ratios of the main inverter in the latch of the SSA so as to convert the analog MDQ voltage to full rail digital data. This circuit will begin a writeback operation sooner in a 2-cycle writeback cycle, and accordingly is faster (and also denser) than the circuit of Figure 2, but may not be able to write complete rail voltages to the bitlines. This circuit also receives assistance from the SSA as feedback

from MDQGATE to MDQ assists in the writeback operation, and moreover device T50 is no longer required.

[0043] The present invention changes the timing of the wordline WL to effect an efficient refresh for a direct sense, destructive-read sensing scheme. For a normal prior art read and write cycles, the wordline WL is active for one cycle for a read operation and one cycle for a write operation, with an interim restore between the read and write operations. In contrast thereto, in the present invention, for a refresh cycle, the wordline active time is altered and remains active for 2-cycles with no interim reset.

[0044] The subject invention restores cell data by first sensing bitline data with a PSA sensing circuit without a storage means, and then transfers the data to a latch in the SSA which is common to a group of direct sense memory arrays. A single MDQ master data line is used to first carry the read data as an analog level which is passed to the SSA, and then after it is digitized, the digitized data is returned on the same MDQ global data line as a full-rail digital signal back to the memory array bitlines.

[0045] The disclosed circuits and timing sequences read the data with the PSA and transfer the data to a shared SSA along a shared MDQ global data line, and convert the analog data to digital data with an isolation device and a latch with weak feedback. The resistive isolation device T2 and the read current supply from the devices T25/T4 are then shut off, after which the feedback device T50 is enabled to pass the inverted and amplified data back to the array cell on the shared data line.

[0046] The present invention improves the write cell levels. As shown by the original sense signal levels and the refresh/writeback signal levels of Figure 4, the refresh operation strengthens the cell data beyond the normal write cell levels, because a 2-cycle write/refresh operation provides more write time to writeback a more complete data level into the memory cell.

[0047] The read/writeback scheme is used as the primary writeback mechanism in a destructive read memory array where 2-cycles are used for each memory read cycle. The first cycle is a read cycle, and the second cycle is a writeback operation as described. The 2-cycle destructive read architecture eliminates the need for a cache and complex caching algorithms.

[0048] The direct sense array can be used instead of an SRAM cache as in the prior art to hold refresh data, and eliminates the area penalty and complexity of an SRAM cache for a direct sensed eDRAM memory array. In destructive read arrays with caches, the writeback and refresh architecture of the present invention allows the destructive read arrays to be refreshed while the cache is performing other unrelated tasks.

[0049] While several embodiments and variations of the present invention for a writeback and refresh circuitry for direct sensed DRAM macro are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.